International Journal of Electrical and Computer Engineering (IJECE)
Vol. 8, No. 6, December 2018, pp. 4880~4891
ISSN: 2088-8708, DOI: 10.11591/ijece.v8i6.pp4880-4891

New Dead-Time Compensation Method of Power Inverter Using Carrier Based Sinusoidal Pulse-Width Modulation

Suroso[1], Daru Tri Nugroho[2], Toshihiko Noguchi[3]
[1,2]Electrical Engineering Department, Jenderal Soedirman University, Indonesia
[3]Graduate School of Engineering, Shizuoka University, Japan

Article Info

Article history:

Received Mar 9, 2018
Revised Jul 6, 2018
Accepted Jul 21, 2018

Keyword:

Dead-time
Harmonics
Inverter
Modulation

ABSTRACT

A new dead-time compensation method of power inverter circuits is suggested and presented in this paper. The proposed method utilizes carrier based sinusoidal pulse width modulation technique to produce driving signals of the inverter power switches with dead-time correction capability. The proposed method able to eliminate dead-time effects such as reducing the waveform distortion of the inverter output current, and increasing the fundamental component amplitude of output current. An analysis of the proposed method is presented. Some computer simulations were carried out to investigate the principle operation, and to test performance of the new method. The developed method was validated through experimental test of H-bridge voltage source inverter circuits. The data obtained from the computer simulation and prototype experiments have confirmed that that the proposed method worked well compensating the dead-time in the voltage source power inverter circuits.

Corresponding Author:

Suroso,
Electrical Engineering Department,
Jenderal Soedirman University,
Jl. Mayjen Sungkono km.5, Purbalingga, Jawa Tengah, Indonesia.
Email: suroso.te.unsoed@gmail.com

1. INTRODUCTION

Because of parochial turn-on and turn-off capability of power semiconductor switching devices, a time delay has to be added between the turn-on and turn-off gating signals of the two switching devices in the same leg of a voltage source inverter circuits. This time delay is called as dead-time, which is inherently needed in a voltage source type inverter to avoid short circuits between the switches in the same leg of inverter during switching operation [1]-[4]. The dead-time value depends on type and the power rating of devices used to build the power inverter circuit [5], [6]. The higher the switching speed, a proper dead-time must be properly selected to ensure the inverter circuits works properly [7]. Improper selection of dead-time will cause the inverter fails to work and make damage to the inverter circuits [8].

In fact, the value of dead-time is comparatively small if compared to the fundamental period of current or voltage waveform. However, in a voltage-source power inverter, the cumulative dead-time in one cycle will give significant negative effect such as increasing waveform distortion of the output current and voltage, reducing the fundamental amplitude of output voltage and currents, and making the phase error [9]-[11]. When an ac motor is supplied by a voltage source power inverter, the stator voltages of the motor will contain harmonics generated by dead-time effect. The motor operation will be badly influenced by these harmonics, particularly at no-load and low frequencies operations, making more losses of machine, reducing efficiency and make torque pulsation of the motor [12], [13].

The additional motor losses and torque ripple depend on the harmonic level of the voltage and current supplied by the power inverter [14], [15]. For amplifier application, the dead-time generates more distortions

of the output waveform [16]. In the renewable energy application, especially in a grid connected power inverter, the harmonics of the inverter's AC output current will also be transferred into the AC power grid [17]. The harmonics will pollute the AC power grid and power load. Hence, reduction, elimination and compensation are required to prevent the negative effects of dead-time in a power inverter's driving signals.

Some methods have been developed and presented by many researchers to eliminate and counterbalance the effects of dead-time**.** Basically, the traditional dead-time counterbalance methods of inverter can be classified into two major types depending on the manner of dead-time effects addressed. In the first type, the averaging theory is used. In this technique, the total dead-time effects in one cycle of the modulating waveform is reviewed [18]-[20]. However, in this method, the speed of the compensating process is slightly slow. For the second method, the compensation is conducted on a single pulse basis, per time-switching rate, hence the compensation speed can be faster and more accurate [21], [22].

However, in these conventional techniques, the dead-time compensation is accomplished either by decreasing or increasing the width of driving pulses of the inverter's power switches, based on the current polarity of the inverter. Therefore, in these methods the current sensing becomes very important [23]. The polarity detection of the current waveform is very crucial round zero crossing to make the dead-time effect compensation works effectively. To address this issue, some dead-time compensating methods apply algorithms for current estimation as discussed in references [24], [25], [26] and [27]. However, these techniques operate effectively only at low modulation index or low current condition. In the low modulation index, it is possible to modify the pulse-width of the inverter gating signals without reaching the minimum or maximum pulse width signals. Accurate small-signal model of the voltage source power inverter circuits which includes model non-linearities as well as modulation and dead-time effects is very important in this method [28].

In this research publication, a different dead-time compensation method suitable for voltage source type inverter circuits is explained. The proposed method based on carrier based sinusoidal pulse width modulation (CSPWM) strategy with level-shifted. The principle operations of the proposed new method are presented and discussed. Validation through the computer simulations were conducted for the three-level voltage source inverter. Furthermore, the proposed compensation method was implemented to the prototype of three-level H-bridge voltage source inverter.

2. PROPOSED DEADTIME COMPENSATION METHOD

Figure 1(a) shows the conventional level shifted CSPWM with two triangular carrier waveforms, V_{cr1} and V_{cr2}. These carrier signals have the same frequency, the same phase and the same peak-to-peak amplitude. The carrier signals frequency sets the switching frequency of power switches used in the inverter [29], [30]. The waveform V_m is the sinusoidal modulating signal. Its frequency gives the main frequency of the inverter output voltage waveform. This modulation method is commonly used for gating signals generation of a three-level inverter [31], [32]. For the multilevel power inverter circuits with higher level number of output voltage waveform, more triangular carriers are required with different offset values [33], [34]. In practical, for all voltage source power inverter circuits, a dead-time is added to the generated signals to drive the power semiconductor switches.

In order to compensate the effect of dead-time, Figure 1(b) is the suggested the level shifted CSPWM with dead-time compensating function. The visible difference compared to the conventional carrier-based level shifted SPWM is the existence of intersection area between the upper and lower carrier signals. This crossing area is not available in the conventional modulation method in Figure 1(a).

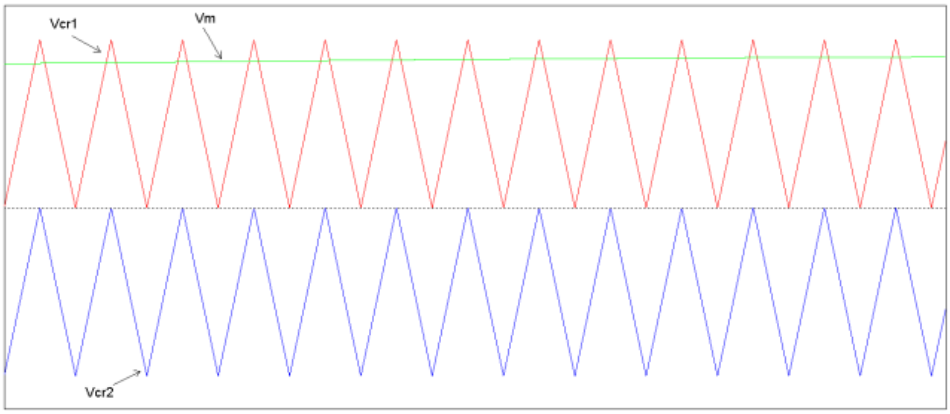
To make a clear analysis, an enlarged figure of the proposed modulation technique with compensating capability of dead-time is presented in Figure 2. This figure depicts detail operation of the proposed new dead-time compensating method. The voltage $\mathbf{V_c}$ is the triangular carrier waveform of the conventional CSPWM. In the conventional modulation strategy, the minimum and maximum peak of the triangular carrier waveform does not cross the intersection area, $\mathbf{A_c}$. In another word, there is no part of a triangular carrier crossing each other. The signal $\mathbf{V_m}$ is the modulating signal which is the sinusoidal waveform. Its frequency is usually much lower than the carrier waveforms. Comparing the triangular carrier and modulating signals in the comparator circuits will generate the PWM signal patterns for the power inverter gating signals. In this figure, the voltage signal $\mathbf{V_c'}$ is the triangular carrier waveform implementing compensation of dead-time. In this modulation technique, there is a part of the carrier waveforms crossing each other in the intersection area indicated by $\mathbf{A_c}$. If the percentage of the crossing area denoted as **C**, we can write:

$$C = A_c / A \quad (1)$$

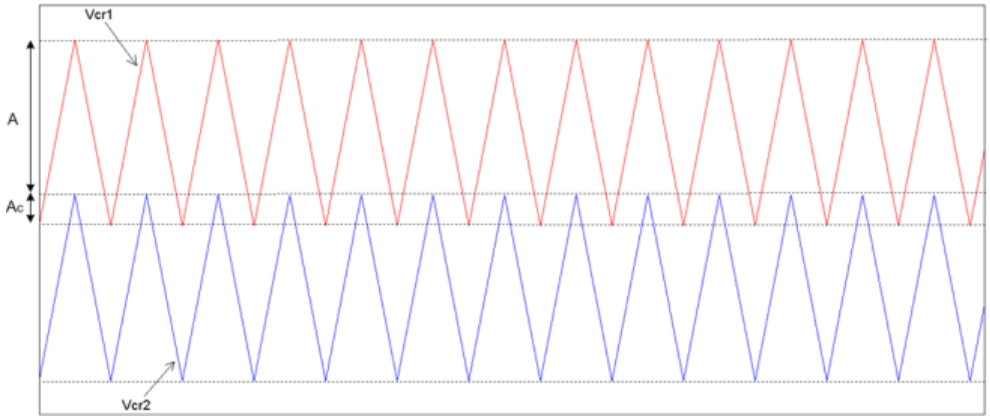
Where $\mathbf{A_c}$ is the magnitude of the crossed carrier waveform, and **A** is the rest magnitude of the carrier as shown in Figure 1(b) and Figure 2. The $\Delta \boldsymbol{T}$ is the dead-time value added to gating signal **S**. This dead-time causes voltage signal losses indicated as $\Delta \boldsymbol{V}$. If the inverter switching frequency is $\boldsymbol{f}$, the total voltage drop in one cycle output voltage is:

$$V_D = 2.f.\Delta V \quad (2)$$

Where, $\boldsymbol{V_D}$ is the total voltage drop produced by the dead-time in one cycle PWM output voltage. In one cycle of switching frequency, there will be a turn-on and a turn-off transition. Consequently, the higher the switching frequency will cause a larger voltage drop.



(a)



(b)

Figure 1. (a) Conventional level shifted CSPWM, (b) proposed level shifted CSPWM with dead-time compensating function

In Figure 2, the gating signal with dead-time compensating capability is the **S'**. It is generated by the proposed modulation technique. The dead-time value is the same as Δ**T**. However, the great point in this picture is that the voltage signal losses generated by the dead-time is compensated using the suggested modulation. The compensating voltage pulse compensated by the dead-time compensation is indicated as Δ**V'**. Utilizing the compensation method, the compensated output voltage $\mathbf{V_o'}$ will be the same to the ideal output voltage. The voltage losses produced by the dead-time will not be generated.

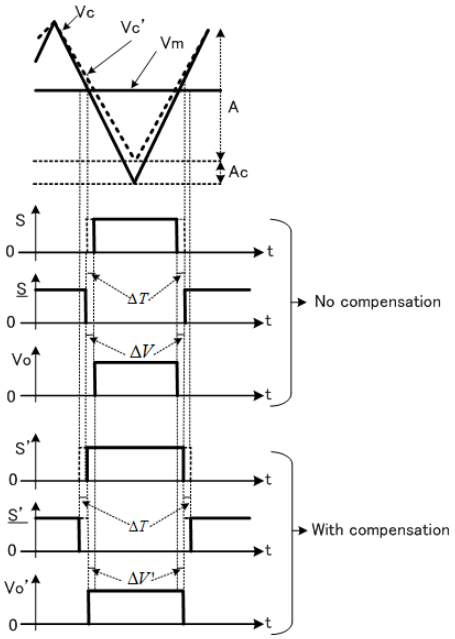


Figure 2. Basic principle of the suggested method.

3. COMPUTER SIMULATION TEST RESULTS

Computer simulations were conducted to examine the proposed modulation method using software power PSIM. The three-level H-bridge voltage source inverter circuit as shown in Figure 3 was tested. The parameter tests are listed in Table 1. A 100 V DC voltage was used as the input power source of the inverter circuits. The switching frequency was chosen as 22 kHz in order to push the switching harmonic components into higher region and to prevent audible noise. The dead-time value was 3.5μs. Inductive power load with series resistance R 20 Ω and inductor 3 mH was connected to the inverter. The fundamental output voltage frequency was 60 Hz.

Figure 4 shows the test results using computer simulation of the three-level H-bridge inverter presenting the waveforms of load current and output voltage when the modulation index was 0.9 with no compensation. The harmonic spectra of the load current and PWM output voltage are described in Figure 5(a) and Figure 5(b). Furthermore, Figure 6 presents simulation test results of the load current and voltage waveform when the compensation method was implemented. The intersection area of the carrier signals was set to be 9%. The harmonic spectra of load current and voltage waveform are shown in Figure 7(a) and Figure 7(b), successifely. Figure 8 denotes a relation between the intersection area value of triangular carrier waveforms, ***C***, and the total harmonic distortion (THD) of the load current waveform for the three-level H-bridge inverter. The lowest current distortion value is achieved at intersection area value around 9%. This value is used in the computer simulation and laboratory prototype experimental test.

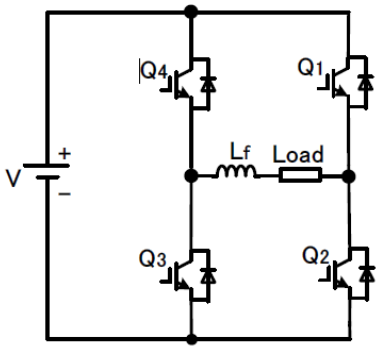


Figure 3. H-bridge inverter circuits [30]

Table 1. Computer simulation test parameters

Variable	Value
DC input voltage	100 V
Inverter switching frequency	22 kHz
Dead-time value	3.5μs
Power load	R = 20Ω, L =3mH
Fundamental output voltage frequency	60 Hz

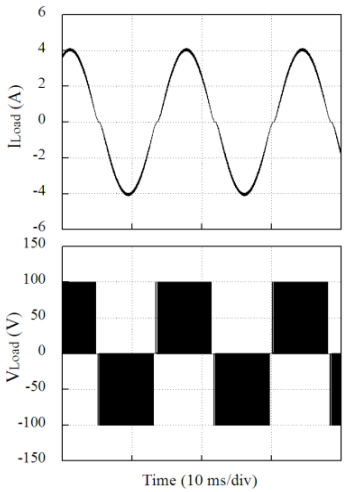
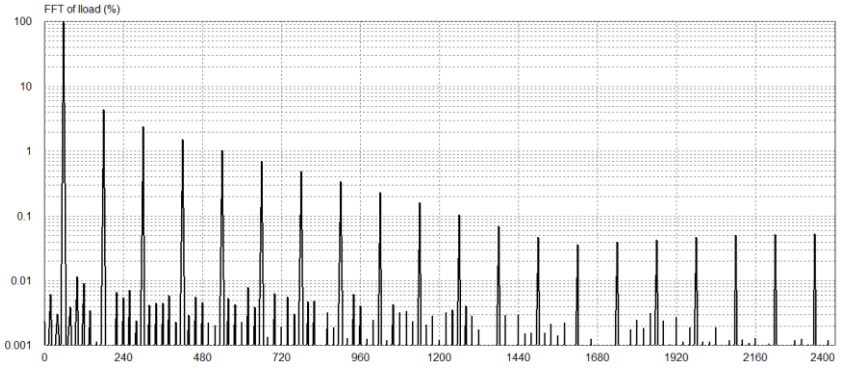
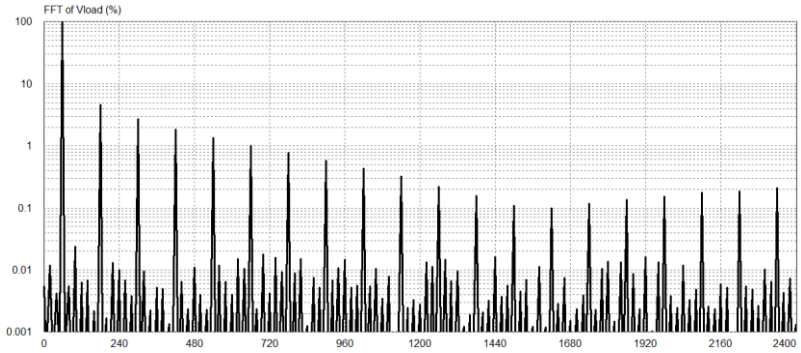


Figure 4. Load current and voltage waveforms of H-bridge voltage source inverter with no compensation



(a)



(b)

Figure 5. (a) Harmonic spectra of load current waveform without compensation, (b) harmonic spectra of voltage waveform without compensation.

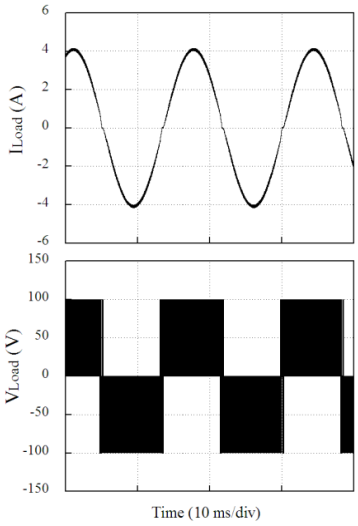
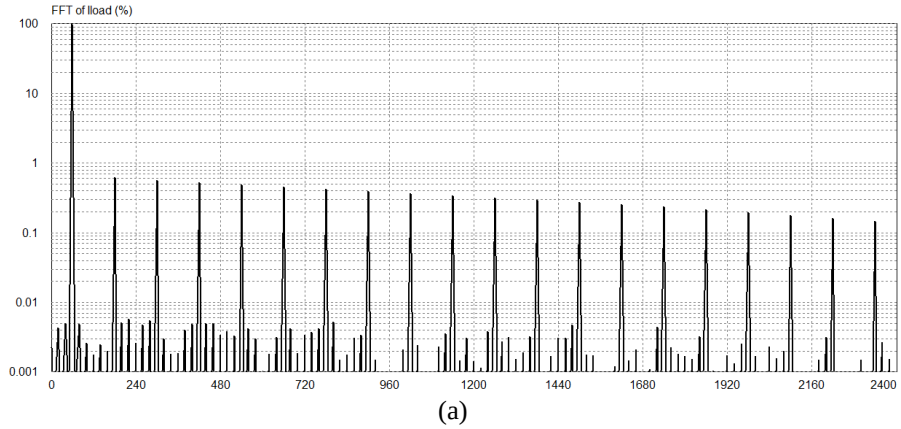
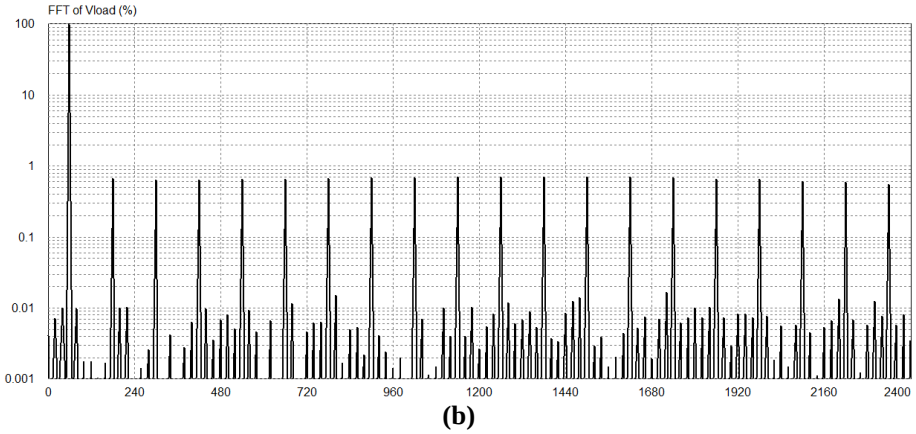


Figure 6. Load current and voltage waveforms of H-bridge voltage source inverter with proposed method



(a)



(b)

Figure 7. (a) Harmonic spectra of load current with compensation, (b) harmonic spectra of output voltage with compensation

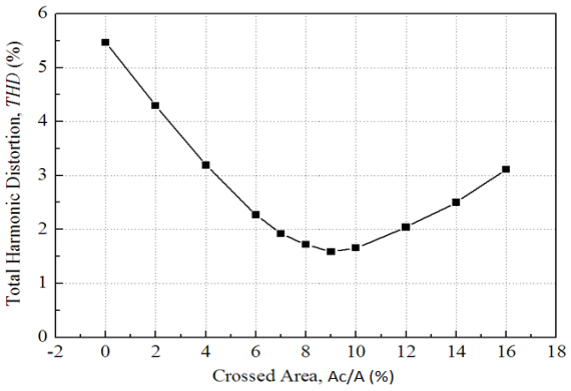


Figure 8. A relation between crossed area of the triangular carriers and THD of output current

Figure 9 represents the comparison of pulse-width of PWM output voltage waveform for the ideal waveform (no dead-time), with dead-time but no compensation, and with dead-time equipped with proposed compensation method. As can be observed in this figure, the suggested method recovered the loss of pulse-width of PWM output voltage to the ideal waveform. Figure 10 presents the simulation results of a comparison harmonic orders in case of using compensation and without compensation. The results show that the magnitudes of the low frequency harmonics become much lower by implementing the dead-time compensation method.

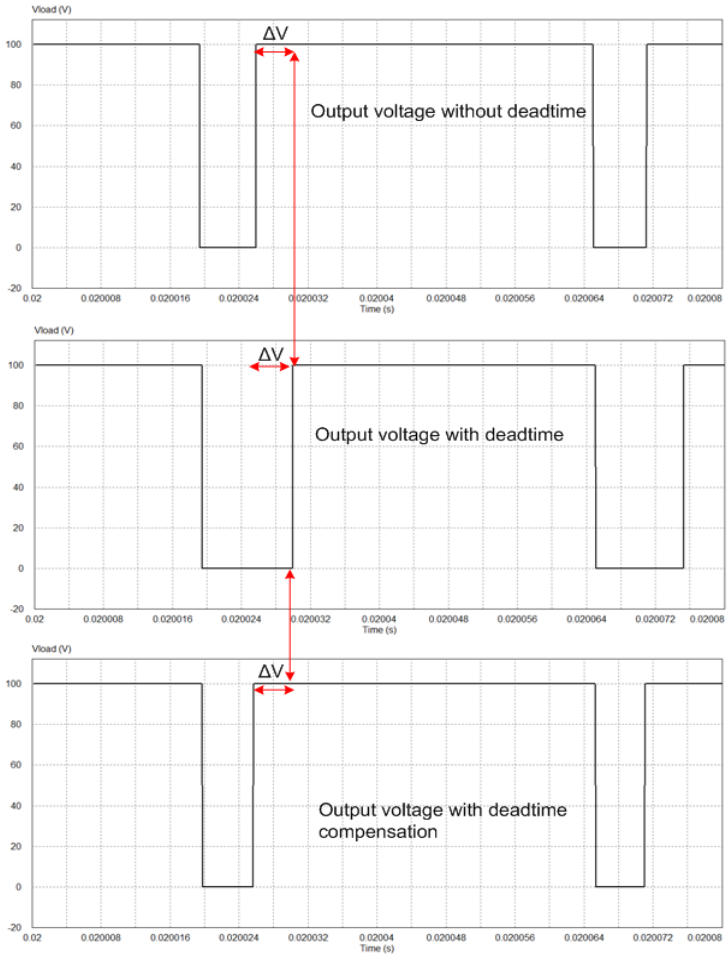


Figure 9. Enlarged pulse width of PWM output voltage waveform in case of no dead-time (ideal waveform), with dead-time but no compensation, and compensated pulse

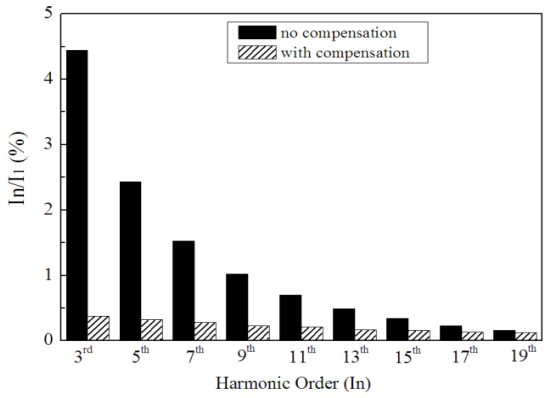


Figure 10. A comparison of output current harmonic components of H-bridge voltage source inverter (computer simulation test result)

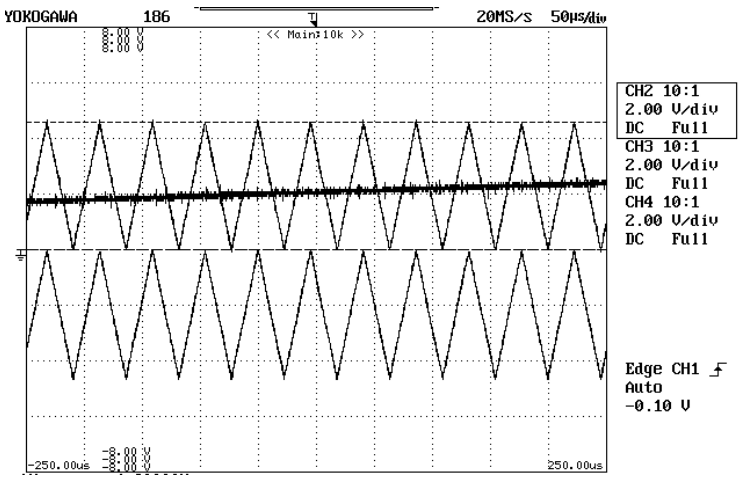
4. EXPERIMENTAL TEST RESULTS

Validation and verification of the proposed method experimentally were done in laboratory. A laboratory prototype of the H-bridge voltage source power inverter was made using power MOSFET FK30SM-6. This section presents laboratory experimental test results of the proposed new dead-time compensation technique. Table 2 lists the experimental test parameters of the inverter prototype. A 50 V DC voltage power source was used in the inverter prototype experiment. Figure. 11(a) shows the measured triangular carriers and sinusoidal modulating waveform of the conventional SPWM with no compensation. Whereas, Figure 11(b) presents the measured triangular and sinusoidal signals of the suggested compensation method. The intersection area of the triangular carrier waveforms is chosen as 9%, which is the optimal value for the output current distortion as determined in the previous computer simulation test results. Figure 12 is measured dead-time added to the inverter gating signals. The measured dead-time was 3.5 µs.

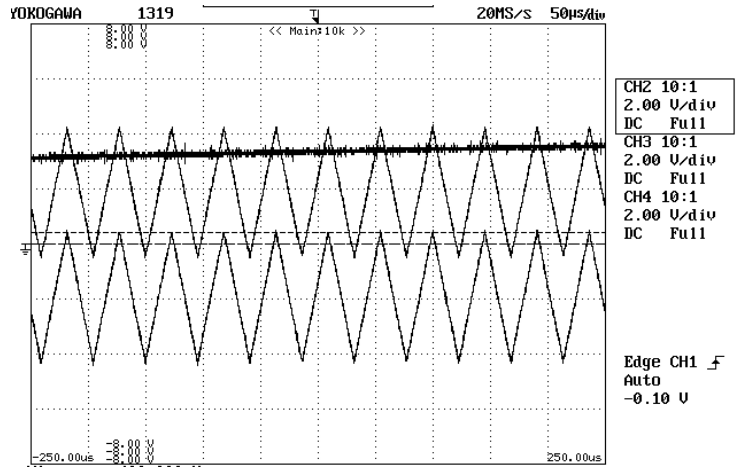
Figure 13(a) displays the measured waveforms of the PWM AC voltage and load current in case of no dead-time compensation. A distortion caused by the deadtime effect can be observed in the load current waveform. Figure 13(b) presents the PWM voltage and load current waveforms of the H-bridge inverter when the proposed method was employed. The load current was almost a pure sinusoidal waveform with lower distortion. Furthermore, Figure 14 shows the more detail comparison of the low frequency harmonics in case of no compensation, and when compensation was employed. The data were obtained by laboratory experimental test. Experimentally, it confirmed that the new compensating method of dead-time worked well eliminating dead-time effect, reducing the harmonic distortion produced by the dead-time.

Table 2. Experimental test parameters

Variable	Value
DC input voltage	50 V
Inverter switching frequency	22 kHz
Dead-time value	3.5µs
Load	R = 20 Ω, L =3mH
Main frequency of output voltage	60 Hz



(a)



(b)

Figure 11. (a) The triangular carrier and sinusoidal modulating waveforms of SPWM in case of without dead-time compensation, (b) The triangular carrier and sinusoidal modulating waveforms of SPWM in case of with dead-time compensation

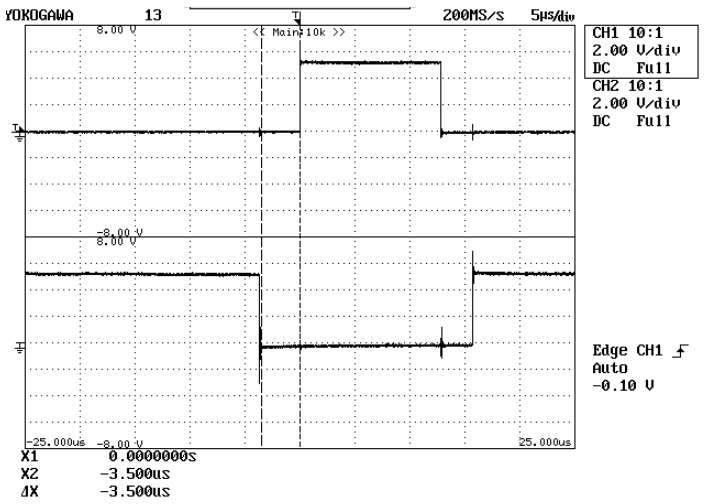
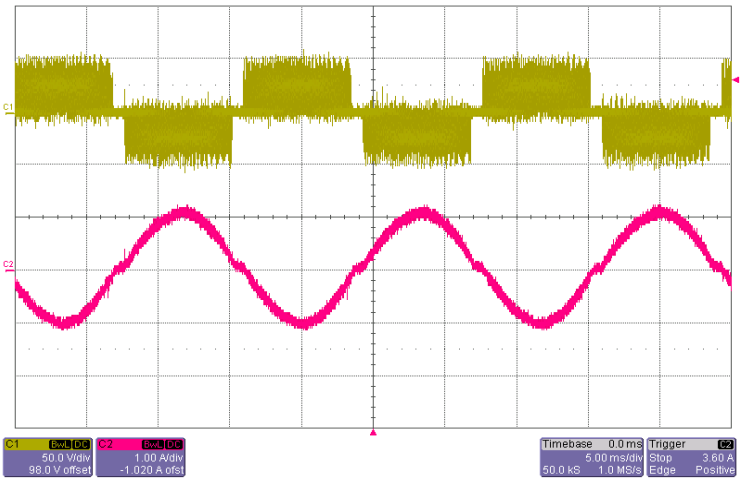
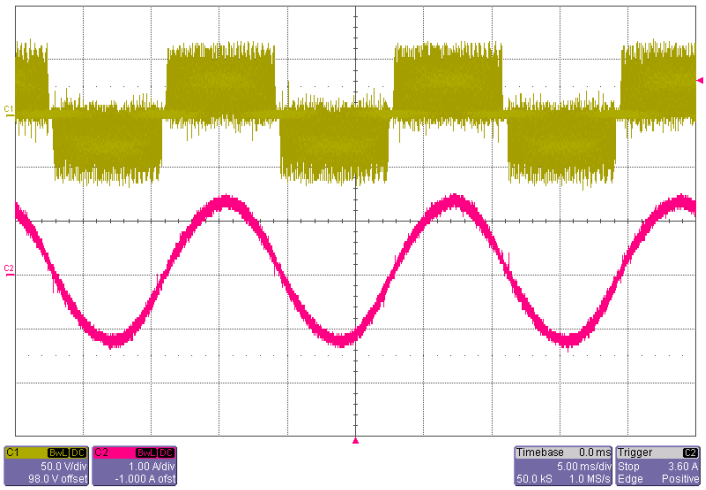


Figure 12. Dead-time of the inverter gating signal



(a)



(b)

Figure 13. (a) Measurement result of output voltage and load current waveforms in case of no compensation, (b) The measured waveforms of voltage and load current when compensation was applied

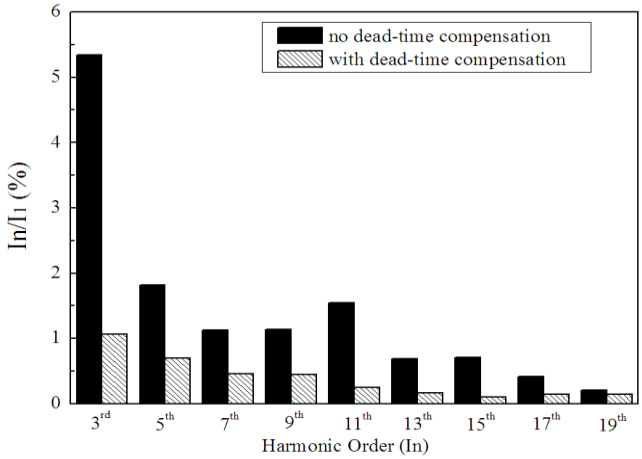


Figure 14. Comparison of current harmonic components of H-bridge inverter in case of no compensation and with compensation (experimental test result)

5. CONCLUSION

Dead-time is inherently needed in voltage source inverter circuits to stave off short circuit conditions between the lower and upper switches of inverter's power switches at the same inverter leg. Adding dead-time in the driving signals of the inverter power switches will increase harmonic components of current and voltage produced by inverter. Compensating the dead-time effects is mandatory to make inverter works properly. A different dead-time effect compensation technique of the voltage source inverter using triangular CSPWM was presented and discussed. The new compensation method has been confirmed and validated by using computer simulations and experimentally in laboratory. The proposed method works properly eliminating the dead-time impact in a power inverter

REFERENCES

[1] Y. Murai, *et al.*, "Waveform distortion and correction circuit for PWM Inverters with switching lag-times," *IEEE Transaction on Industrial Applications.*, vol. 23, pp. 881–886, Sept./Oct. 1987.

[2] C. M. Wu, *et al.*, "Analytical Technique for Calculating the Output Harmonics of an H-Bridge Inverter with Dead Time," *IEEE Transaction on circuits and systems*, vol. 46, no. 5, pp. 617-627, May 1999.

[3] J. Choi, *et al.*, "Inverter output voltage synthesis using novel dead time compensation", *IEEE Transaction Power Electronics*, vol. 11, no. 2, pp. 221-227, March 1996.

[4] R. Mu˜noz, *et al.*, "On-Line Dead-Time Compensation Technique for Open-Loop PWM-VSI Drives," *IEEE Transaction on Power Electronics*, vol. 14, no. 4, pp. 683 – 689, 1999.

[5] Y. Tadano, *et al.*,"A Multilevel PWM Strategy Suitable for high voltage motor direct drive systems in consideration of the adverse effect of deadtime," *IEEJ Transaction on Industry Application*, vol. 126, no. 1, p.p. 1-9, 2006.

[6] J. Choi, S *et al.*, "Inverter output voltage synthesis using novel dead time compensation," in *Proc. IEEE Applied Power and Electronics Conf., 1994*, pp. 100–106.

[7] A. C. Oliveira, *et al.*, "Improved Dead-Time Compensation for Sinusoidal PWM Inverters Operating at High Switching Frequencies," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2295-2304, 2007.

[8] S. Hong, *et al.*, "Dead-time compensation and realization method for 3-level NPC Inverter," *IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific)*, 2014, p.p. 1-5.

[9] D. Leggate, *et al.*, "Pulse-Based Dead-Time Compensator for PWM Voltage Inverters," *IEEE Transactions on Industrial Electronics*, vol. 44, No. 2, p.p. 191-197, April 1997.

[10] L. Chen, *et al.*, "Dead-time elimination for voltage source inverters", *IEEE Transaction on Power Electronics*, vol. 23, no. 2, pp. 574-580, March 2008.

[11] J. Sabate, *et al.*, "Dead-time Compensation for a High-Fidelity Voltage Fed Inverter," *Proceeding of IEEE Power Electronics Specialists Conference*, 2008, p.p. 4419-4425.

[12] H. Kim, *et al.*, "On-Line Dead-Time Compensation Method Based on Time Delay Control," *IEEE Transaction on control system technology*, vol. 11, no. 2, pp. 279-285, 2003.

[13] C. Attaianese, *et al.*, " Predictive Compensation of Dead-Time Effects in VSI Feeding Induction Motors," *IEEE Transaction on Industry Applications*, vol. 37, no. 3, pp. 856-863, May/June 2001.

[14] N. Urasaki, *et al.*, "An Adaptive Dead-Time Compensation Strategy for Voltage Source Inverter Fed Motor Drives," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1150-1160, September 2005.

[15] Guha, *et al.*,"Small-Signal Stability Analysis of an Open-Loop Induction Motor Drive Including the Effect of Inverter Deadtime," *IEEE Transactions on Industry Applications*, vol. 52, issue 1, pp. 242-253, 2016.

[16] Poon, *et al.*, "A ZVS PWM converter for a full audio band amplifier," in *Proc. 27th IEEE Power Electronics Specialists Conf.*, Baveno, Italy, June 1996, pp. 1261–1265.

[17] S. B. Kjaer, *et al.*, "A review of single-phase grid connected inverters for photovoltaic modules", *IEEE Transaction on Industry Application*, vol. 41, no. 5, p.p. 1292-1306, September/October 2005.

[18] S. H. Hwang, *et al.*, "Dead time compensation method for voltage-fed PWM inverter", *IEEE Transaction Energy Conversion*, vol. 25, no. 1, pp. 1-10, March 2010.

[19] D. H. Lee, *et al.*, "A simple and direct dead-time effect compensation scheme in PWM-VSI", *IEEE Transaction on Industry Application*, vol. 50, no. 5, pp. 3017-3025, Sep. 2014.

[20] Z. Guo, *et al.*, "Inverter Dead-Time Compensation and Control Scheme for Reducing Harmonic Distortion and Improving Conversion Efficiency," *IEEJ Transaction on Industry Applications*, vol. 130, issue 1, pp. 26-36 2010.

[21] C. D. Townsend, *et al.*, "Deadtime compensation for Model Predictive Control of Power Inverters," *IEEE Transaction on Power Electronics*, vol. 32, issue. 9, p.p. 7325 – 7337, 2017.

[22] N. Hur, *et al.*," A Two-Degrees-of-Freedom Current Control Scheme for Deadtime Compensation," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 3, pp.557-564, 2000.

[23] J. Lin, "A New Approach of Dead-Time Compensation for PWM Voltage Inverters," *IEEE Transaction on circuits and systems*," Vol. 49, No. 4, pp. 476-483, 2002.

[24] L. Ben-Brahim, *et al.*, "Implementation of iterative learning control based dead-time compensation for PWM inverters," *In Proc. of 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, p.p. 1-5.

[25] Kuznietsov, *et al.*, "Model predictive control of a voltage source inverter with compensation of deadtime effects," *IEEE International Conference on Industrial Technology (ICIT)*, 2015, p.p. 2532-2536.

[26] M. Yang, *et al.*, "A Novel Dead-Time Compensation Method for Direct Predictive Control,"*Fifth International Conference on Instrumentation and Measurement, Computer, Communication and Control (IMCCC)*, 2015, p.p. 273-277.
[27] Imura, *et al.*,"Dead-Time Compensation in Model Predictive Instantaneous-current Control,"*in proc. of The 38th Annual Conference on IEEE Industrial Electronics Society (IECON 2012)*, Canada, 2012, pp. 1-6.
[28] S. Ahmed, *et al.*, "Small-Signal Model of Voltage Source Inverter (VSI) and Voltage Source Converter (VSC) Considering the DeadTime Effect and Space Vector Modulation Types," *IEEE Transactions on Power Electronics*,vol 32, Issue 6, pp. 4145 – 4156, June 2017.
[29] Suroso, and T. Noguchi, "Five-Level Common-Emitter Inverter using Reverse-Blocking IGBTs", *TELKOMNIKA (Telecommunication Computing Electronics and Control)*, vol. 9, No.3, p.p. 1693-6930, December 2011.
[30] Suroso, A. Mubyarto, and T. Noguchi, "A Different Single-Phase Hybrid Five-Level Voltage-Source Inverter Using DC-Voltage Modules", *TELKOMNIKA (Telecommunication Computing Electronics and Control)*, vol. 12, no.3, pp. 557-562, September 2014.
[31] L. M. Tolbert, *et al.*, "Multilevel PWM Methods at Low Modulation Indices", *IEEE Transaction on Power Electronics*, vol.15, no.4, pp. 719-725, 2000.
[32] F. Gao, *et al.*, "Topological Design and Modulation Strategy for Buck–Boost Three-Level Inverters", *IEEE Transaction on Power Electronics*, vol.24, no.7, p.p. 1722-1732, 2009.
[33] Suroso, A. N. Aziz, and T. Noguchi, "Five-level PWM Inverter with a Single DC Power Source for DC-AC Power Conversion", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 8, pp. 1230-1237, September 2017.
[34] N. Thombre, R. S. Rawat, P. Rana, Umashankar S, "A Novel Topology of Multilevel Inverter with Reduced Number of Switches and DC Sources", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 5, no.1, p.p. 56-62, July 2014.

BIOGRAPHIES OF AUTHORS

Suroso received the B. Eng. degree in electrical engineering, from Gadjah Mada University, Indonesia in 2001, and the M. Eng. degree in electrical and electronics engineering from Nagaoka University of Technology, Japan in 2008. He was a research student at electrical engineering department, Tokyo University, Japan from 2005 to 2006. He earned the Ph.D degree in energy and environment engineering department, Nagaoka University of Technology, Japan in 2011. He was a visiting researcher at electrical and electronics engineering department, Shizuoka University, Japan from 2009 to 2011. Currently, He is an associate professor at department of electrical engineering, Jenderal Soedirman University, Purwokerto, Jawa Tengah, Indonesia. His research interest includes power converters, and its application in renewable energy conversion.

Daru Tri Nugroho received bachelor (B.Eng.) degree in electrical engineering from Institute Teknologi Sepuluh November, Surabaya, Indonesia and M.Eng. degree in electrical engineering from Universitas Indonesia. Currently He is a lecturer in Electrical Engineering Department, Jenderal Soedirman University. His research interests are power electronics and renewable energy system.

Toshihiko Noguchi was born in 1959. He received the B. Eng. degree in electrical engineering from Nagoya Institute of Technology, Nagoya, Japan, and the M. Eng. and D. Eng. degrees in electrical and electronics systems engineering from Nagaoka University of Technology, Nagaoka, Japan, in 1982, 1986, 1996, respectively. In 1982, he joined Toshiba Corporation, Tokyo, Japan. He was a Lecturer at Gifu National College of Technology, Gifu, Japan, from 1991 to 1993 and a Research Associate in electrical and electronics systems engineering at Nagaoka University of Technology from 1994 to 1995. He was an Associate Professor at Nagaoka University of Technology from 1996 to 2009. He has been a Professor at Shizuoka University since 2009. His research interests are static power converters and motor drives. Dr. Noguchi is a Member of the IEE-Japan and a Senior Member of the IEEE.